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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHOI, WOO H	
ART UNIT	**PAPER NUMBER**
2186	12

DATE MAILED: 04/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,459	GEFEN ET AL.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10,11,13-15 and 19-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10,11,13-15 and 19-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

"the executing entity 30" in lines 14 and 15 on page 10 should be changed to "the executing entity 12".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 10, 11, 13 – 15, and 19 – 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 10 , and 15 recite the limitation "via an interface separate from said standard memory interface". Applicant points to Figure 2 and the unlabeled arrow and the use of the term "architecture" on page 10, as support for this new limitation. However, there is no indication that this figure represents hardware architecture as argued by Applicant. The specification specifically discloses, in line 3 on page 5, that "FIGURE 2 is an illustration of the process".

4. Claims 11, 13, 14, and 19 – 24 are rejected for including the deficiencies of their parent claims.

5. Claims 23 and 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The claims recite the limitation "**physically** separate executable memory components". The section of the specification that Applicant recites for support, page 10 line 19 through page 11 line 2, does not support the limitation. While the specification discloses a set of buffers, it does not disclose that they are physically separate components.

6. Claim 25 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The claimed limitation "executable memory component receiving said stored code from said non-executable memory component independently of said executing entity" is not supported by the specification. An arrow from the NAND array 30 to the buffers 20 shown on figure 2 does not support this limitation. The only thing that can be inferred from the diagram is the

direction of the download. Again, contrary to Applicant's assertion, the specification specifically states that "FIGURE 2 is an illustration of the process".

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 10 – 11, 13 – 15, 19 – 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Microsoft (Windows 95 Resource Kit) in view of Johnson *et al.* (US Patent No. 5,987,536, hereinafter "Johnson").

9. With respect to claims 10, Microsoft discloses a device for enabling an executing entity of a host system to execute code, comprising:

(i) a non-executable memory component, for storing the code (page 70, hard-disk); and

(ii) at least one executable memory component (page 69, RAM, see also page 975, memory is organized as pages and segments of 64K), each said executable memory component for presenting at least a portion of said stored code to the executing entity in a manner that enables the executing entity to execute said portion of said stored code directly from said each executable memory via a standard memory interface (programs are directly executed in RAM),

each said executable memory component receiving said stored code from said non-executable memory component, and

(iii) a mechanism for indicating availability, in one of said at least one executable memory component, of code requested by the executing entity (page 975 – 976, memory paging).

However, Microsoft does not specifically disclose that the executable memory component receives said stored code via an interface separate from said standard memory interface. On the other hand, Johnson specifically discloses a PC architecture that runs Windows operating system with a standard interface (Johnson, figure 3, 42) and another interface (figure 3, 50) where the executable component (48) receives stored code in a non-executable memory (30) via another interface (50).

It would have been obvious to one of ordinary skill in the art, having the teachings of Microsoft and Johnson before him at the time the invention was made, to combine the Windows operating system teachings of Microsoft in the computer system of Johnson that runs Microsoft Windows operating system to gain better understanding of both the software and hardware aspects of the system so that the system can be administered, managed and used more effectively.

10. With respect to claim 11, the non-executable memory component and said at least one executable memory components are separate from the host system (pages 69 – 70, CPU, hard disk and RAM are separate from the CPU).

11. With respect to claim 13, the device comprises a plurality of said executable memory components (page 976, pages in physical memory), such that while one said executable memory component is presenting a first said at least portion of said stored code to the executing entity, a second said at least portion of said stored code is being downloaded to another said executable memory component (page 974 – 976, process scheduling and multitasking and memory paging).

12. With respect to claim 14 each said at least one executable memory component is too small to accommodate all of the code at once (pages 69 – 70, System Requirements for Windows 95, Windows 95 requires more disk space for all of its code than RAM, see also memory paging on pages 975 – 976, one segment is 64K bytes).

13. With respect to claim 15, Microsoft discloses a method of executing code, comprising the steps of (a) storing the code in a non-executable memory component (pages 974 – 976, Process Scheduling and Multitasking and Memory Paging);

(b) downloading only a first portion of the code from said non-executable memory component to a first executable memory component (page 975, demand paging only loads a portion of the executable file from to disk to RAM);

(c) executing said downloaded code, by an executing entity of a host system, directly from said executable memory component via a standard memory interface, said first executable memory component being separate from said host system (hard disk and RAM are separate from CPU);

(d) subsequent to said downloading, requesting code to be executed, by said executing entity;

(e) if said requested code is outside of said downloaded first portion of the code:

(i) downloading a second portion of the code, including said requested code, from said non-executable memory component to said first executable memory component; and

(ii) during said downloading of said second portion of the code, suspending activity of said executing entity (As noted above, in demand paging, pages are moved in and out of RAM as needed. While a page is being loaded in to the physical memory, or RAM, a process cannot continue as it does not have the needed page available in the physical memory).

However, Microsoft does not specifically disclose that the downloading from said non-executable memory component to said first executable memory component is via an interface separate from said standard memory interface. On the other hand, Johnson specifically discloses a PC architecture that runs Windows operating system with a standard interface (Johnson, figure 3, 42) and another interface (figure 3, 50) where the executable component (48) receives stored code in a non-executable memory (30) via another interface (50).

It would have been obvious to one of ordinary skill in the art, having the teachings of Microsoft and Johnson before him at the time the invention was made, to combine the Windows operating system teachings of Microsoft in the computer system of Johnson that runs Microsoft Windows operating system to gain better understanding of both the software and hardware aspects of the system so that the system can be administered, managed and used more effectively.

14. With respect to claim 19, wherein said suspending includes supplying a busy signal to said executing entity (While Microsoft does not specifically mention a "busy signal", an equivalent functionality is required to let the operating system know that the requested page is available so that the process can be resumed).

15. With respect to claim 20, the method further comprises the steps of:

(d) downloading a second portion of the code to a second executable memory component; and

(e) executing said downloaded second portion of the code, by said executing entity (See page 976, virtual to physical mapping diagram. Multiple pages are loaded in and out of RAM).

16. With respect to claim 21 said second executable memory component is separate from said host system (RAM is separate from CPU).

17. With respect to claim 22, said executing entity executes said downloaded second portion of the code directly from said second executable memory component (executable programs are executed directly from the physical memory).

18. With respect to claims 23 and 24, the executable memory components are physically separate executable memory components (Microsoft, page 976, pages in the physical memory are separate from each others).

19. With respect to claim 25, as Applicant stated in the amendment the main difference between this claim and claim 10 is that claim 25, states that the executable memory component receives the stored code from the non-executable independently of the executing entity. Microsoft and Johnson disclose all of the limitations of claim 10 as discussed above. Figure 3 of Johnson's disclosure clearly shows that the path between the disk and memory is via the PCI bus, which is independent of the host bus 42. Also note that 52 includes a direct memory access (DMA) controller.

20. Claims 10 – 11 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Hwang (US Patent No. 6,263,399).

21. With respect to claims 10, Hwang discloses a device for enabling an executing entity of a host system to execute code (figure 2), comprising:

(i) a non-executable memory component (26), for storing the code (col. 1 lines 15 – 23); and

(ii) at least one executable memory component (col. 6, lines 23 – 28), each said executable memory component for presenting at least a portion of said stored code to the executing entity in a manner that enables the executing entity to execute said portion of said stored code directly from said each executable memory (RAM is a executable memory and the data or code from the NAND flash memory is presented to the CPU in the CPUs native form just like any other directly executable memories, see col. 5, lines 20 – 24) via a standard memory interface (figure 2, interface between the CPU 10 and the memory interface 24), each said executable memory component receiving said stored code from said non-executable memory component (NAND flash memory 26) via an interface separate from said standard memory interface (interface between 26 and 24); and

(iii) a mechanism for indicating availability, in one of said at least one executable memory component, of code requested by the executing entity (col. 1, lines 28 – 35).

22. With respect to claim 11, said non-executable memory component and said at least one executable memory component are separate from the host system (24 and 26 are separate from the CPU 10).

23. With respect to claim 14, each said at least one executable memory component is too small to accommodate all of the code at once (col. 6, lines 24 – 27).

Response to Arguments

24. Applicant's arguments with respect to the above claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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April 27, 2004

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